

**REMARKS**

In the Office Action mailed August 16, 2006, the Examiner rejected claims 1-19 under 35 U.S.C. § 103(a). Applicants have amended claim 1 to clarify that the buried insulation layer is directly over the semiconductor substrate. No new matter has been added. Applicants submit that claims 1-19 are in condition for allowance and respectfully request notice to this effect.

**I. Response to the Rejections under 35 U.S.C. § 103(a) Based on Librizzi/Shirato**

The Examiner rejected claims 1, 2, 5, 6, 9, 10, 13, 14, and 17 under 35 U.S.C. § 103(a) as being obvious in view of the combination of U.S. Patent No. 6,429,502 ("Librizzi") and Japanese Publication No. 02271567 ("Shirato"). In amended claim 1, Applicants recite an integrated circuit having a semiconductor substrate, a buried insulation layer directly over the semiconductor substrate, a semiconductor mesa over the buried insulation layer, and a guard ring substantially surrounding the semiconductor mesa. The guard ring extends through the buried insulation layer contacting the semiconductor substrate.

Neither Librizzi, nor Shirato teach an integrated circuit having a guard ring as claimed. The Examiner stated, and Applicants agree, that Librizzi fails to disclose a guard ring that extends through the buried insulation layer contacting the semiconductor substrate. (Office Action, page 3.) The Examiner also stated that "Shirato discloses a semiconductor device that has a guard ring (6B) that extends through the buried insulation layer (3) contacting the semiconductor substrate (1)." To understand the teachings of Shirato, Applicants have obtained an unofficial translation of Shirato, which is included as an attachment to this response.

While Shirato describes a guard ring that contacts the semiconductor substrate, Shirato's guard ring does not extend through a buried insulation layer directly over the semiconductor substrate. Instead, Shirato describes an impurity region 2 located between an insulating film 3 and a first semiconductor substrate 1. (See, e.g., Shirato, Abstract.) Thus, Shirato's guard ring extends through the insulating film 3 and the impurity region 2 to contact the semiconductor substrate.

This impurity region 2 is necessary to Shirato's device. The impurity region 2 is used to form capacitors with the first semiconductor substrate 1. (See, e.g., Translation, page 6.) As described by Shirato, "the necessary capacitors for analog circuits" are formed on another substrate than the substrate on which the analog and digital circuits are formed. (See, e.g., Translation, page 2.) Thus, Shirato does not suggest forming the buried insulation layer directly over the semiconductor substrate. Because of this and other design differences, devices formed on Shirato's second semiconductor substrate 4 will be subjected to more noise than the devices formed in Applicants' claimed semiconductor mesa.

Because neither Librizzi nor Shirato show or suggest a guard ring that extends through the buried insulation layer directly over the semiconductor substrate, Applicants submit that claim 1 is not obvious in view of the combination of Librizzi and Shirato. Claims 2, 5, 6, 9, 10, 13, 14, and 17 depend from claim 1. Accordingly, Applicants also submit that claims 2, 5, 6, 9, 10, 13, 14, and 17 are not obvious in view of the combination of Librizzi and Shirato for at least the reasons described above with reference to claim 1.

In light of the above, Applicants respectfully request withdrawal of these rejections under 35 U.S.C. § 103(a).

**II. Response to the Rejections under 35 U.S.C. § 103(a) Based on Librizzi/Shirato/Beyer**

The Examiner rejected claims 3, 4, 7, 8, 11, 12, 15, and 16 under 35 U.S.C. § 103(a) as being obvious in view of the combination of Librizzi, Shirato, and U.S. Patent No. 5,264,387 ("Beyer"). Claims 3, 4, 7, 8, 11, 12, 15, and 16 depend from claim 1. As described above, neither Librizzi nor Shirato show or suggest a guard ring that extends through the buried insulation layer directly over the semiconductor substrate. The Examiner cited to Beyer for the teaching of a semiconductor device that has a semiconductor mesa that comprises a silicon mesa. (Office Action, page 4.) However, this teaching of Beyer does not overcome the deficiencies identified with respect to Librizzi and Shirato. Accordingly, Applicants submit that claims 3, 4, 7, 8, 11, 12, 15, and 16 are not obvious in light of the combination of Librizzi, Shirato, and Beyer for at least the reasons described above with reference to claim 1.

In light of the above, Applicants respectfully request withdrawal of these rejections under 35 U.S.C. § 103(a).

**III. Response to the Rejections under 35 U.S.C. § 103(a) Based on Librizzi/Shirato/Hirabayashi**

The Examiner rejected claims 18 and 19 under 35 U.S.C. § 103(a) as being obvious in view of the combination of Librizzi, Shirato, and U.S. Patent No. 5,889,314 ("Hirabayashi"). Claims 18 and 19 depend from claim 1. As described above, neither Librizzi nor Shirato show or suggest a guard ring that extends through the buried insulation layer directly over the semiconductor substrate. The Examiner cited to Hirabayashi for the teaching of a semiconductor device that has a metal guard ring. (Office Action, page 5.) However, this teaching of Hirabayashi does not overcome the

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deficiencies identified with respect to Librizzi and Shirato. Accordingly, Applicants submit that claims 18 and 19 are not obvious in light of the combination of Librizzi, Shirato, and Hirabayashi for at least the reasons described above with reference to claim 1.

In light of the above, Applicants respectfully request withdrawal of these rejections under 35 U.S.C. § 103(a).

### CONCLUSION

In light of the above amendments and remarks, Applicants submit that the present application is in condition for allowance and respectfully request notice to this effect. The Examiner is requested to contact Applicants' representative below if any questions arise or she may be of assistance to the Examiner.

Respectfully submitted,

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